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Amendments to the Specification:

Please add the following new paragraphs after the paragraph ending at page 4, line 12, and before the heading "BRIEF DESCRIPTION OF DRAWINGS":

According to another aspect of the invention, there is a method of generating digital traffic for use in testing a multi-port communication device. The method comprises the steps of: generating a reference digital traffic pattern; generating a plurality of traffic streams replicated from the reference digital traffic pattern, wherein the plurality of traffic streams are used for loading respective input ports of the communication device; and introducing a plurality of phase delays among the plurality of traffic streams when compared to the reference digital traffic pattern. Transmission of one traffic stream of the plurality of traffic streams has a phase delay determined from a length of a buffer associated with the one traffic stream, and traffic streams begins at a time between boundaries of time units of a transmission rate associated with the one traffic stream.

The phase delay may be determined from the length of the buffer and the transmission rate. The communication device may effect statistical multiplexing amongst the plurality of traffic streams. The plurality of traffic streams may be continuous digital data streams. The plurality of traffic streams may be ATM cell streams.

Another traffic stream of the plurality of traffic streams may have a second phase delay determined from a length of a second buffer associated with the another traffic stream and the transmission rate.

According to another aspect of the invention, there is a method of loading a multi-port communication device with digital traffic. The method comprises the steps of: generating a digital traffic pattern; and providing a plurality of streams replicated from the digital traffic pattern to input ports of the communication device. The plurality of streams has a plurality of phase delays therebetween. Transmission of at least one stream of the plurality of streams begins at a time between boundaries of time units of a

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transmission rate associated with the each of the digital traffic pattern, and have a phase delay determined by at least a length of a buffer associated with the at least one stream. The communication device may effect statistical multiplexing of the plurality of streams.

According to another aspect of the invention, there is provided a method of loading a multi-port communication device with digital traffic. The method comprises the steps of: generating from a digital traffic stream with a plurality of digital traffic streams having identical data content thereto; and providing the plurality of digital traffic streams with a plurality of phase delays therebetween to input ports of the communication device. Each phase delay is related to a buffer length. The phase delay is determined from a ratio utilizing the length of the buffer associated with at least one of the plurality of traffic streams. Transmission of at least one of the plurality of digital traffic streams begins at a time between boundaries of time units of a transmission rate associated with the each of the digital traffic. The communication device may effect statistical multiplexing of the plurality of digital traffic streams.

According to another aspect of the invention, there is a method of operating a digital traffic replicating device for use in testing a multi-port communication device. The method comprises the steps of: receiving an input digital traffic stream; and generating a plurality of output digital traffic streams from the input digital traffic stream. A phase delay is introduced to at least one stream of the plurality of output digital traffic streams. The phase delay is determined from a ratio utilizing a buffer length associated with at least one stream. Transmission of the at least one of the plurality of output digital traffic streams begins at a time between boundaries of time units of a transmission rate associated with the input digital traffic stream. The plurality of output digital traffic streams have traffic patterns that are replicas of the input digital traffic stream. The communication device may effect statistical multiplexing of the plurality of output digital traffic streams.

According to another aspect of the invention, there is an apparatus for generating digital traffic for use in testing a multi-port communication device. The apparatus comprises: a reference pattern generator generating a reference pattern defining a digital

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traffic pattern; a traffic stream replicating device generating a plurality of traffic streams replicated from the reference pattern; and a phase delay module providing respective phase delays among the plurality of traffic streams utilizing a series of buffers. Transmission of at least one traffic stream of the plurality of traffic streams is provided with a phase delay based on a length of a buffer of the buffers associated with the at least one traffic stream, and begins at a time between boundaries of time units of a transmission rate associated with the plurality of traffic streams. The plurality of traffic streams load respective input ports of the communication device.

The each phase delay may be determined from the length of the buffer and the transmission rate. The communication device may effect statistical multiplexing of the plurality of traffic streams. The plurality of traffic streams may be continuous digital data streams. The plurality of traffic streams may be ATM cell streams.

According to another aspect of the invention, there is an apparatus for loading a multi-port communication device with digital traffic. The apparatus comprises: a traffic generator generating input digital traffic; and a traffic manager providing a plurality of streams replicated from the input digital traffic to input ports of the communication device. One stream of the plurality of streams has a phase delay being determined from a length of a buffer associated with the one stream such that transmission of the one stream begins at a time between boundaries of time units of a transmission rate associated with the input digital stream.

The communication device may effects statistical multiplexing of the plurality of streams and the phase delay may determined from a ratio utilizing the length of the buffer associated with the each stream and the transmission rate.

According to another aspect of the invention, there is provided an apparatus for loading a multi-port communication device with digital traffic. The apparatus comprises: a traffic generating module generating from a digital traffic stream a plurality of digital traffic streams having identical data content thereto; and a traffic manager providing the plurality of digital traffic streams to input ports of the communication device with a phase

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delay introduced to at least one of the plurality of digital traffic streams being determined from a buffer length and a transmission rate associated with the at least one of the plurality of digital traffic streams. Transmission of the at least one of the plurality of digital traffic streams begins at a time between boundaries of time units of a transmission rate associated with the input digital traffic. The communication device may effect statistical multiplexing of the plurality of digital traffic streams.

According to another aspect of the invention, there is provided a digital data stream replicating device. The device comprises: an input port for receiving an input continuous digital data stream comprising input data blocks at an input transmission rate; a traffic replicator to replicate the input continuous digital data stream into N streams of replicated continuous digital data streams; N output ports for transmitting the plurality of replicated continuous digital data streams at output transmission rates, each output transmission rate at least equal to the input transmission rate; and a delay module providing a predetermined delay for each replicated continuous digital data stream of the plurality of replicated digital data streams with respect to the input continuous digital data stream. Transmission of at least one stream of the each replicated continuous digital data stream has a phase delay determined from a length of a buffer associated with at least one stream and begins at a time between boundaries of time units of a transmission rate associated with the input digital traffic.

The device may further include an idle block generator for introducing idle data blocks into a replicated continuous digital data stream of the plurality of replicated continuous digital data streams for transmission through an output port of the N output ports when an output transmission rate associated with the output port is greater than the input transmission rate.

The delay module may comprise: a memory having N first-in first-out (FIFO) logical buffers established therein, each logical buffer being associated with one digital data stream of the plurality of replicated continuous digital data streams. When a logical buffer of the N FIFO logical buffers is full, data blocks associated with the logical buffer are forwarded to an output port of the N output ports associated with the logical buffer.

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The delay module comprises: a memory having N first-in first-out (FIFO) logical buffers established therein, each logical buffer being associated with one digital data stream of the plurality of replicated continuous digital data streams. When a logical buffer of the N FIFO logical buffers is full, data blocks associated with the logical buffer are forwarded to an output port of the N output ports associated the logical buffer, such that the delay provided to a digital data stream transmitted through the output port correlates to a length of the logical buffer and its associated transmission rate.

The delay module for each replicated continuous output digital data stream may forward data blocks associated with its logical buffer at the output transmission rate of the corresponding output port; and the delay provided to the replicated continuous digital data stream may correlate to a transmission rate of the corresponding output port.

Each of the logical buffers may be established by copying the input data blocks into a physical buffer organized in the memory, and each of the logical buffers may be corresponding to a different physical buffer. The logical buffers may be established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer. The input and transmitted digital data streams may be ATM cell streams.

According to another aspect of the invention, there is provided a digital data stream replicating device for providing data traffic input patterns to a communication device. The device comprises: an input port for receiving a continuous digital data stream comprising input data blocks at an input transmission rate; a memory; N output ports, each having an output transmission rate at least equal to the input transmission rate; a traffic processor connected between the input port and the N output ports, providing N first-in first-out logical buffers in the memory and associating each of the input data blocks of the continuous digital data stream with each one of the N logical buffers so as to replicate the input data blocks thereacross, each logical buffer being associated with only one of the output ports; and a scheduler to forward data blocks associated with a given logical buffer through its corresponding output port when the given logical buffer is full. Transmission of the data blocks begins at a time between boundaries of time units

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of a transmission rate associated with the corresponding output port and a phase delay associated with the transmission of the data block is determined from at least a length of the logical buffer.

Each logical buffer may have a length selected to achieve a relative delay between the input digital data stream and an output digital data stream may be replicated by the logical buffer for its corresponding output port.

Each of the logical buffers may be established by copying the input data blocks into a physical buffer organized in the memory, and each of the logical buffers may correspond to a different physical buffer. The logical buffers may be established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer. The input and output digital data streams may be ATM streams.

The device may further include an idle traffic generator for introducing empty data blocks into an output digital data stream replicated by the logical buffer for its corresponding output port when the output transmission rate of its corresponding output port is greater than the input transmission rate.

For each logical buffer, its length and the output transmission rate of its corresponding output port may be selected to achieve a relative delay between the input digital data stream and an output digital data stream may be replicated by the logical buffer for its corresponding output port. The input and output digital data streams may be ATM streams.

According to another aspect of the invention, there is provided a performance testing device. The device comprises: a traffic generator for generating a continuous digital data stream; an input port for receiving the continuous digital data stream at an input transmission rate; a broadcaster for replicating the input digital data stream N times; N output ports for transmitting each such replicated digital data stream through a separate output port at an output transmission rate at least equal to the input transmission rate; and a delay module for introducing a predetermined relative delay for each the transmitted

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digital data stream with respect to the input digital data stream. Transmission of at least one stream of the each the transmitted digital data stream begins at a time between boundaries of time units of a transmission rate associated with the each transmitted digital data stream and has a phase delay determined by at least a length of a buffer associated with the at least one stream.

In another aspect of the invention, there is provided a performance testing device. The device comprises: a traffic generator for generating a continuous digital data stream; an input port for receiving the continuous digital data stream comprising input data blocks at an input transmission rate; a memory; N output ports, each having an output transmission rate at least equal to the input transmission rate; a traffic processor connected between the input port and the N output ports providing N first-in first-out logical buffers in the memory and associating each of the input data blocks of the continuous digital data stream with each one of the N logical buffers so as to replicate the input data blocks thereacross, each logical buffer being associated with only one of the output ports; and a scheduler for forwarding data blocks associated with a given logical buffer through its corresponding output port when the given logical buffer is full. Transmission of the data blocks begins at a time between boundaries of time units of an output transmission rate associated with transmission of the data blocks, and the transmission has a phase delay determined by at least a length of the logical buffer.

According to another aspect of the invention, there is provided a performance testing device. The device comprises: a traffic generator for generating a continuous digital data stream; an input port for receiving the continuous digital data stream comprising input data blocks at an input transmission rate; a memory; N output ports, each having an output transmission rate at least equal to the input transmission rate; a traffic processor connected between the input port and the N output ports for establishing N first-in first-out logical buffers in the memory, and associating each of the input data blocks of the continuous digital data stream with each one of the N logical buffers so as to replicate the input data blocks thereacross, each logical buffer being associated with only one of the output ports; and a scheduler for forwarding data blocks associated with a

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given logical buffer through its corresponding output port when the given logical buffer is full. Transmission of the data blocks begins at a time between boundaries of time units of an output transmission rate associated with transmission of the data blocks. One of the N first-in first-out logical buffers is a given size and at least another of the N first-in first-out logical buffers is a different size than the given size.

The device may further include an idle block generator to introduce idle data blocks into an output digital data stream replicated by the logical buffer for its corresponding output port when the output transmission rate of its corresponding output port is greater than the input transmission rate.

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